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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,778	03/06/2002	Robin Alexis Takasugi	10018457-1	8925

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EXAMINER	
CORRIELUS, JEAN M	
ART UNIT	**PAPER NUMBER**
2162	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,778	TAKASUGI ET AL.	
	Examiner	Art Unit	
	Jean M. Corrielus	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the pre-appeal conference filed on November 25, 2005, in which claims 1 and 3-24 are presented for further examination.

Response to Arguments

2. Applicant's arguments filed on November 25, 2005 with respect to Gharachorloo's reference have been fully considered but they are not persuasive However, the arguments with respect to the 35 USC 112, first paragraph are not persuasive. The rejection of the last office action with respect to Gharachorloo's reference has been withdrawn.

Remark

3. Applicant asserted that table 1 of the specification clearly discloses multiple registers and the use of such registers is described in the specification page 3, lines 9 to page 7, line 20. It is clearly submitted that table 1 of the applicant's disclosure provides multiple registers and wherein said registers are detailed in the specification, page 3, lines 9 to page 7, line 20. However, the portion of the disclosure as indicated by the applicant does support the invention as claimed in claims 1 and 3-24. Although, the applicant shows support of the words increment and decrement (see specification, page 9, lines 21-32 and page 11, lines 6-8). However, such portions of the specification do not actually support applicant's claimed language. There is a big different between the cited portion of the applicant's disclosure and the recited claimed language. Claim 1, however, recites "storing in a first register a value for tracking a number of data units that have been transferred into a buffer----". According to the specification page 6, lines 18-25, the register

does not actually store any value for tracking the number of data units that have been transferred into a buffer. In fact, it is the data mover 500 that keeps track the progress of the transfer by managing the counter 502, which is decremented by the value of the block sector after each successful block transfer from the host to the buffer. So after each unit of data transferred between the transfer system and the host, all the registers are updated. There is no indication showing the value of a register is modified based on a transfer of a data unit into a buffer nor a value storing in a second register to increment the value contained in the first register. Applicant's disclosure, page 9, lines 21-23, states after the signal 509 is received by the data mover 500, the value of register 502 is decreased by 1 and the value of register 505 is increased by 1. There is no mentioned as to whether the value in register 502 is incremented based on the value contained in the register 505.

Applicant's disclosure, page 11, lines 6-8, states after the signal 509 is received by the data mover 500, the value of register 503 is decreased by 1 and the value of register 505 is increased by 1. There is no mentioned as to whether a value is stored in register 505 to decrement the value in the register 502; and the value in register 502 is decremented based on the value contained in the register 505.

There is nowhere in applicant disclosure showed as to whether to store an address in the fourth and fifth register representing the location in the buffer where data is being transferred. There is also no functional relationship between elements in the claim.

There is nowhere in applicant disclosure showed as to whether to store an address in the sixth register representing a beginning of the buffer, nor storing an address in a seventh register

representing an end of the buffer. There is also no functional relationship between elements in the claim.

There is nowhere in applicant disclosure showed as to whether to store a value in the eighth register representing a storage capacity of the buffer.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

While transferring data between a host device and a storage medium could be considered a tangible result, the body of claims 1, 10, 19 and 22 do not appear to actually support the preamble by including a step or steps, which accomplish that act. There is no functional relationship between the body of the claims 1, 10, 19 and 22 and the preamble.

In claim 1, after the command to transfer data received from the host device, there was actually no transfer took place. Claim 1 recites that "storing in a first register a value for tracking a number of data units that have been transferred into a buffer----". According to the specification page 6, lines 18-25, the register does not actually store any value for tracking the number of data units that have been transferred into a buffer, in fact the data mover 500 keeps track the progress of the transfer by managing the counter 502, which is decremented by the value of the block sector after each successful block transfer from the host to the buffer. So after

each unit of data transferred between the transfer system and the host, all the registers are updated. There is no indication showing the value of a register is modified based on a transfer of a data unit into a buffer nor a value storing in a second register to increment the value contained in the first register. Applicant's disclosure, page 9, lines 21-23, states after the signal 509 is received by the data mover 500, the value of register 502 is decreased by 1 and the value of register 505 is increased by 1. There is no mentioned as to whether the value in register 502 is incremented based on the value contained in the register 505.

The limitations of claim 3 are not supported by Applicant disclosure. Applicant's disclosure, page 11, lines 6-8, states after the signal 509 is received by the data mover 500, the value of register 503 is decreased by 1 and the value of register 505 is increased by 1. There is no mentioned as to whether a value is stored in register 505 to decrement the value in the register 502; and the value in register 502 is decremented based on the value contained in the register 505.

The limitations of claim 4 are not supported by Applicant disclosure. There is nowhere in applicant disclosure mentioned as to whether to store an address in the fourth and fifth register representing the location in the buffer where data is being transferred. There is also no functional relationship between elements in the claim.

The limitations of claim 5 are not supported by Applicant disclosure. There is nowhere in applicant disclosure mentioned as to whether to store an address in the sixth register representing a beginning of the buffer, nor storing an address in a seventh register representing an end of the buffer. There is also no functional relationship between elements in the claim.

The limitations of claim 6 are not supported by Applicant disclosure. There is nowhere in applicant disclosure mentioned as to whether to store a value in the eighth register representing a storage capacity of the buffer.

Claims 10-17 contain the deficiency as listed in the claims 1-6 above. Therefore, claims 10-17 are rejected using the same rationale as applied to claims 1-6 above.

Claims 19-24 contain the deficiency as listed in the claims 1-6 above. Therefore, claims 19-24 are rejected using the same rationale as applied to claims 1-6 above. In addition, claims 19 and 22 recite "a buffer's fullness". It is unclear to one having ordinary skill in the art as what applicant means by "buffer's fullness".

Claim 22 recites the limitation "the buffer's fullness" in line 5. There is insufficient antecedent basis for this limitation in the claim.

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 and 3-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 1, after the command to transfer data received from the host device, there actually no transfer is taking place. Claim 1 recites that "storing in a first register a value for tracking a number of data units that have been transferred into a buffer----". According to the

specification page 6, lines 18-25, the register does not actually store any value for tracking the number of data units that have been transferred into a buffer, in fact the data mover 500 keeps track the progress of the transfer by managing the counter 502, which is decremented by the value of the block sector after each successful block transfer from the host to the buffer. So after each unit of data transferred between the transfer system and the host, all the registers are updated. There is no indication showing the value of a register is modified based on a transfer of a data unit into a buffer nor a value storing in a second register to increment the value contained in the first register. Applicant's disclosure, page 9, lines 21-23, states after the signal 509 is received by the data mover 500, the value of register 502 is decreased by 1 and the value of register 505 is increased by 1. There is no mentioned as to whether the value in register 502 is incremented based on the value contained in the register 505. Claim 1 recites "storing in a first register a value for tracking a number of data units tat have been transferred into a buffer but that have not yet been transferred out of the buffer". Such limitation is not supported by the specification.

The limitations of claim 3 are not supported by Applicant disclosure. Applicant's disclosure, page 11, lines 6-8, states after the signal 509 is received by the data mover 500, the value of register 503 is decreased by 1 and the value of register 505 is increased by 1. There is no mentioned as to whether a value is stored in register 505 to decrement the value in the register 502; and the value in register 502 is decremented based on the value contained in the register 505.

The limitations of claim 4 are not supported by Applicant disclosure. There is nowhere in applicant disclosure mentioned as to whether to store an address in the fourth and fifth register

representing the location in the buffer where data is being transferred. There is also no functional relationship between elements in the claim.

The limitations of claim 5 are not supported by Applicant disclosure. There is nowhere in applicant disclosure mentioned as to whether to store an address in the sixth register representing a beginning of the buffer, nor storing an address in a seventh register representing an end of the buffer. There is also no functional relationship between elements in the claim.

The limitations of claim 6 are not supported by Applicant disclosure. There is nowhere in applicant disclosure mentioned as to whether to store a value in the eighth register representing a storage capacity of the buffer.

Claims 10-17 contain the deficiency as listed in the claims 1-6 above. Therefore, claims 10-17 are rejected using the same rationale as applied to claims 1-6 above.

Claims 19-24 contain the deficiency as listed in the claims 1-6 above. Therefore, claims 19-24 are rejected using the same rationale as applied to claims 1-6 above. In addition, claims 19 and 22 recite "a buffer's fullness". Applicants are advised to amend the specification or cancel the above-mentioned limitations from the claims. Applicants are reminded that new matter should be added.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1 and 3-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter, specifically, as directed to an abstract idea.

While transferring data between a host device and a storage medium could be considered a tangible result, the body of claims 1, 10, 19 and 22 do not appear to actually support the preamble by including a step or steps, which accomplish that act. Additionally, the claims 1, 3-24 appear to define non-statutory processes because they merely manipulate an abstract idea without a claimed limitation to a practical application. The language of the is not tied to an environment or machine which would result in a practical application that produce a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. claims 1 and 10, 19 and 22 recite a series of steps without producing a concrete result. It does not appear to be anything subjective to raise an issue with whether theses steps produce a concrete result.

The dependent claims 3-9, 20-21 and 23-24 are rejected for fully incorporating the errors of their respective base claims by dependency.

Claims 18 and 22 define non-statutory processes because they merely recite a software application not execute by a computer medium for transferring data between the host device and the storage medium. Such ASIC software application is not part of the host device for performing the act of transferring data. Claims 18 and 22 define an abstract idea without a claimed limitation to a practical application. The language of the is not tied to an environment or machine which would result in a practical application that produce a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. Applicant is advised to amend the claims by specifying the claim being directed to a practical application and producing a tangible result ***being executed*** by a general-purpose computer in order to correct the above indicated deficiencies.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Siegel US Patent no.5, 261,072.

As to claim 1, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out the buffer" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "modifying the value contained in the first register in response to a transfer of a data unit out of the buffer" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "modifying a value contained in the first register in response to a transfer of a data unit into the buffer" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56).

As to claim 7, Siegel discloses the claimed "wherein the host device is a computer" (col.4, lines 37-50).

As to claim 8, Siegel discloses the claimed "wherein the storage medium comprises non-volatile semiconductor memory" (col.6, lines 15-62).

As to claim 9, Siegel discloses the claimed "implementing the method via an application specific integrated circuit (ASIC) (col.4, lines 1-9; col.7, lines 50-66).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3-6 and 10-24 as best understood by the examiner are rejected under 35 U.S.C. 103(a) as being unpatentable over Siegel US Patent no. 5,261,072 and Sefidvash US Patent no. 5,581,790.

As to claims 3- 6 and 13-17, Siegel discloses the use of storing in the third register a value for incrementing a value contained in the first register" (col.7, lines 33-35); "storing in the register an address representing a location in the buffer where data is being transferred between the buffer and the host device" (col.8, lines 5-65): storing in the register an address representing a location in the buffer where data is being transferred between the buffer and storage medium

(col.8, lines 5-65); storing in a sixth register an address representing a beginning of the buffer (col.8, lines 5-65); storing in the register an address representing and end of the buffer (col.8, lines 5-67) and storing in the register a value representing a storage capacity of the buffer (col.8, lines 5-65). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data. During the course of the data transfer, an integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their

own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claim 10, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "temporarily stores data that is transferred between the host device and the storage medium" (col.3, lines 40-50); "storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out the buffer" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "modifying the value contained in the first register in response to a transfer of a data unit out of the buffer" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "modifying a value contained in the first register in response to a transfer of a data unit into the buffer" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data. During the course of the data transfer, an

integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claim 11, Siegel discloses the claimed "wherein the data transfer system is configured to modify the value contained in the first register in response to a transfer of a data unit between the buffer and the host device" (col.7, lines 33-65; col.8, lines 5-67).

As to claim 12, Siegel discloses the claimed "wherein the data transfer system is configured to modify the value contained in the first register in response to a transfer of a data unit between the buffer and the storage medium" (col.7, lines 33-65).

As to claim 18, Siegel discloses the claimed "implementing the method via an application specific integrated circuit (ASIC) (col.4, lines 1-9; col.7, lines 50-66).

As to claims 19-21, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "storing in a first register a value for determining a buffer's fullness" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "decrementing the value contained in the first register" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "incrementing the value contained in the first register" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel

with the first bits of data. During the course of the data transfer, an integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight register, wherein each one of the registers performs their own special task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claims 22-24, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "temporarily

stores data that is transferred between the host device and the storage medium" (col.3, lines 40-50); "storing in a first register a value for determining a buffer's fullness" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "decrementing the value contained in the first register" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "incrementing the value contained in the first register" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data. During the course of the data transfer, an integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight

register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean M. Corrielus whose telephone number is (571) 272-4032. The examiner can normally be reached on 10 hours shift.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean M Corrielus
Primary Examiner
Art Unit 2162

February 27, 2006